Roll No.

Total Pages: 04

D-180297

B. Tech. EXAMINATION, 2018

Semester V (CBS)

ELECTRONIC LOGIC CIRCUIT DESIGN

EC-503

Time: 3 Hours

Maximum Marks: 60

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note: Attempt *Five* questions in all, selecting *one* question from each Sections A, B, C and D. Section E is compulsory.

Section A

- 1. (a) Explain state diagrams with an example.
 - (b) Draw the logic diagram for a binary up-counter using four JK flip-flops and draw the truth table and the output waveforms.

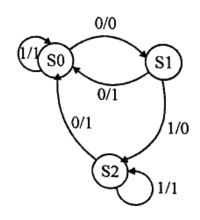
- 2. (a) Design a shift register counter to generate a sequence length of 8 having self-start feature.
 - (b) Design a mod-10 (Decade) synchronous counter using JK flip-flops. 12

Section B

3. A sequential network has one input X and two outputs S and V. X represents a four-bit binary number N, which is input least significant bit first. S represents a four-bit binary number equal to N + 2, which is output least significant bit first. At the time the fourth input is sampled, V = 1, in N + 2 is too large to be represented by four bits; otherwise V = 0

Derive a Mealy state graph and table with a minimum number of states.

4. Design a circuit that implements the state diagram: 12



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Section C

- 5. (a) Design a JK flip-flop asynchronous sequential circuit that has two inputs and single output. The circuit is required to give an output equal to 1 if and only if the same input variable changes two or more times consecutively.
 - (b) Describe cycles in asynchronous sequential circuits.
- 6. (a) Realize the following function using PLA: $f_1(A, B, C) = \sum (0, 2, 4, 5)$ $f_1(A, B, C) = \sum (1, 5, 6, 7)$
 - (b) Derive the PLA program table for a combinational circuit that squares a 3-bit number.Minimize the number of product terms.

Section D

- Design and explain in detail a hazard free asynchronous sequential circuits.
- What are conditions for serial and parallel decomposition in sequential circuits? How serial decomposition affect the functioning of sequential circuit.

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Section E

9. Answer the following:

- $1 \times 12 = 12$
- (a) Distinguish Mealy and Moore machines.
- (b) What is state table?
- (c) What is mean of Modulo Counter?
- (d) Limitation of finite state machines.
- (e) A scynrhonous counter has four flip-flops and the propagation delay of each is 20 ns. What is its maximum counting speed?
- (f) Construct a logic diagram of a clocked D flipflop using AND and NOR gates.
- (g) Describe cycles in asynchronous sequential circuits.
- (h) Explain the difference between stable and unstable states in asynchronous circuits.
- (i) Discuss limitations of FSM with suitable example.
- (j) Briefly describe the FPGA.
- (k) What is the significance of Hazards?
- (1) Parallel decomposition.