[Total No. of Questions - 9] [Total No. of P\ .ed Pages - 2]
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16329(D) - 0 DEC 2016

M. Tech 1st Semester Examination

Computer Architecture & Parallel Processing

CSE1-511

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt five questions in all, selecting only one from each unit. Question No. 9 is compulsory. All questions carry equal marks.

UNIT - I

1. (a) Explain the significance of RTL in the implementation of digital systems.

   (b) Draw the control unit of a basic computer. Show how fetch and decode phases are carried out. (20)

2. (a) How a common bus system can be constructed with multiplexers? Explain with the help of a diagram.

   (b) What are types of shift micro-operation and their uses in programming? (20)

UNIT - II

3. (a) Explain stack based architecture of a CPU with the help of diagram.

   (b) Describe how a vector supercomputer is built on the top of a scalar processor. (20)

4. (a) Explain the Flynn's classification of computer system architecture, providing at least one example of the area of application of each class.

   (b) Explain the architectural distinctions between CISC and RISC processors. (20)

UNIT - III

5. (a) Explain Bernstein conditions based on which two processes can execute in parallel. Detect the parallelism in the following instructions of a program using Bernstein conditions.

   P1: C=D×E

   P2: M=G+C

   P3: A=B+C

   P4: C=L+M

   P5: F=G÷E

   (b) Describe pipelining in VLIW processor. (20)

6. (a) Explain Register Window structure of SPARC architecture.

   (b) Describe Amdahl's Law for speedup performance. (20)

UNIT - IV

7. (a) Explain the arbitration schemes in a backplane bus system.

   (b) Explain the techniques to avoid the pipeline stalling and to minimize pipeline idle time. (20)

8. (a) Compare the relative merits of set-associative and sector-associate cache.

   (b) Describe a four level memory hierarchy technology. (20)

UNIT - V

9. Answer the following briefly:

   (i) Describe massive parallelism for grand challenges.

   (ii) Differentiate between Vector and Symbolic Processors.

   (iii) Explain grain packing approach for parallel programming.

   (iv) Differentiate between Write-through caches and Write-back caches.

   (v) Explain the deadlock avoidance by using virtual channels. (5×4=20)